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| EXAMINER | |
|---|---|
| PIZIALI, JEFFREY J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2673 | 20 |

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/424,544 | INO ET AL. | |
| | Examiner | Art Unit | |
| | Jeff Piziali | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3,5-7,11,13-20,23-29,31,37 and 43-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5-7,11,13-20,23-29,31,37 and 43-48* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 27, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office Action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

2. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

## INFORMATION ON HOW TO EFFECT DRAWING CHANGES

**1. Correction of Informalities -- 37 CFR 1.85**

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

**2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.**

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red

ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

**Timing of Corrections**

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

***Priority***

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Objections***

4. Claim 13 is objected to because of the following informalities: the Amendment filed 26 February 2003 (Paper No. 17) canceled claim 13 (see Pages 1 & 13), but the most recent Amendment filed 20 August 2003 (Paper No. 19) includes a "pending" copy of claim 13 (see Page 4). Appropriate correction is required.

5. Claim 14 is objected to because of the following informalities: claim 14 is dependent upon canceled claim 13 (see above objection to claim 13). Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 3, 5-7, 11, 13-20, 23-29, 31, 37 and 43-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al. (US 4,825,203).

Regarding claim 3, Takeda et al. discloses a liquid crystal display [Fig. 2, 11] comprising a display portion in which a plurality of pixels [Fig. 2, 11-c] are two-dimensionally arranged at intersecting points of gate lines [Fig. 2, 11-a] as many as a plurality of rows and signal lines [Fig. 2, 11-b] as many as a plurality of columns which are wired in a matrix shape; a plurality of driver circuits [Figs. 1(A) & 2, 13 & $q_1$-$q_n$] for applying a signal potential to each pixel in the display portion through the signal lines of the plurality of columns (see Column 2, Line 56 - Column 3, Line 27); and time-divisional switches [Fig. 1(A), 32] for time-divisionally sending a signal potential [Fig. 1(A), $V_R$, $V_G$ & $V_B$] that is outputted from each of the plurality of driver circuits to the signal lines of the plurality of columns, characterized in that a time-dividing number of the time-divisional switches is equal to 3 [see Fig. 1(A), 32], the number of output terminals of each of the plurality of driver circuits is set to a measure [i.e. 1, for instance] of the total number of signal lines [i.e. N] of the plurality of columns, the number of output terminals of each of the plurality of driver circuits is set to a same number, when a size of a frame portion [Fig. 1(A), $q_N$] adjacent to the display portion is specified, the number [i.e. n = 1, for instance] of output terminals of each of the driver circuits is determined on the basis of the specified frame size by the number of lines which can be wired into a wiring region of the frame portion, and when the total number of signal lines of the plurality of columns that is decided by a display system is set to N [Fig. 1(A), $Q_1$ to $Q_N$], the number of the driver circuits is set to N/n [Fig. 1(A), $q_1$ to $q_N$ --

wherein N/1 = N], the total number of signal lines (N > 1) being different than the number (n = 1) of output terminals (see Column 4, Lines 22-68).

Regarding claim 5, Takeda et al. discloses that the number of output terminals of each of the plurality of the driver circuits is set to a power of 2 (i.e. $2^0 = 1$).

Regarding claim 6, Takeda et al. discloses the driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which the display portion is formed (see Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Regarding claim 7, Takeda et al. discloses a memory circuit [Fig. 1(A), 31] for temporarily storing data [Fig. 1(A), D] to be written into the driver circuits; and a control circuit [Fig. 2, 15] for controlling the driver circuits so as to simultaneously write different data from the memory circuit (see Column 3, Lines 8-27 & Column 4, Lines 22-68).

Regarding claim 11, Takeda et al. discloses a leading waveform and a trailing waveform of a signal output waveform [Fig. 1(B), $C_R$, $C_G$ & $C_B$] of each of the plurality of driver circuits are symmetrical with respect to a time base (see Column 4, Lines 47-68).

Regarding claim 13, Takeda et al. discloses a period of time which is selected by the time-divisional switches is equal to or shorter than a third of a horizontal scanning period (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 14, Takeda et al. discloses a leading time and a trailing time of each of the plurality of driver circuits are equal to or shorter than the period of time which is selected by the time-divisional switches (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 15, Takeda et al. discloses a blanking period which is caused for the period of time selected by the time-divisional switches is equal to or shorter than [(a horizontal scanning period) - (the period of time selected by the time-divisional switches x 3)] / 3 (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 16, Takeda et al. discloses the plurality of driver circuits have a function to stop the operation of their output circuit for the blanking period (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 17, Takeda et al. discloses the plurality of driver circuits generate a signal potential so as to correct shift amounts of curves of voltage-transmittance characteristics of red, green and blue [see Fig. 1(A), $V_R$, $V_G$ & $V_B$], by driving the time-divisional switches (see Column 4, Lines 22-46).

Regarding claim 18, Takeda et al. discloses a 1H (H denoting a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by the time-divisional switches is a line of blue, the signal line which is selected at the

second time is a line of green, and the signal line which is selected at the third time is a line of red [see Fig. 4(B); Row i+2 & Columns j, j+1 and j+2].

Regarding claim 19, Takeda et al. discloses a dot inversion driving, the signal line which is selected first by the time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue [see Fig. 5(B); Row i & Columns j, j+1 and j+2].

Regarding claim 20, Takeda et al. discloses time-division of the time-divisional switches distribute signals to red, green and blue constituting one pixel [see Figs. 4(A-B); Column 5, Lines 16-58].

Regarding claim 23, Takeda et al. discloses a surplus connecting region [Fig. 2; 12, 13, & 15] that does not contribute to the display portion [Fig. 2, 11] does not occur on the display (see Column 2, Line 56 - Column 3, Line 27).

Regarding claim 24, Takeda et al. discloses a driver circuit of the plurality of driver circuits is separate and distinct from another driver circuit of the plurality of driver circuits (see Fig. 1(A)).

Regarding claim 25, Takeda et al. discloses a liquid crystal display comprising: a display portion [Fig. 2, 11], the display portion having a plurality of gate lines [Fig. 2, 11-a], a plurality

of signal lines [Fig. 2, 11-b] and a plurality of pixels [Fig. 2, 11-c], a pixel of the plurality of pixels being located at an intersection of a gate line of the plurality of gate lines and a signal line of the plurality of signal lines; and a plurality of driver circuits [Figs. 1(A) & 2, 13, $q_1$-$q_N$], the plurality of driver circuits including at least one general driver circuit [Figs. 1(A), $q_1$ & $q_2$] and one remainder driver circuit [Figs. 1(A), $q_n$], each general driver circuit having a plurality of general driver circuit output terminals [Fig. 1(A), 36], a general driver circuit output terminal of the plurality of general driver circuit output terminals providing a signal potential to one of the plurality of signal lines [Fig. 1(A), Q1 & Q2], the remainder driver circuit having a plurality of remainder driver circuit output terminals [Fig. 1(A), 36], a remainder driver circuit output terminal of the plurality of remainder driver circuit output terminals providing another signal potential to another of the plurality of signal lines [Fig. 1(A), $Q_N$], the quantity [i.e. 2, for instance] of remainder driver circuit output terminals being defined as (S - (OP * (DC-1))), "S" being the quantity of the plurality signal lines [i.e. 5, for instance], "OP" being the quantity of general driver circuit output terminals [i.e. 3, for instance], and "DC" being the quantity of the plurality of driver circuits [i.e. 2, for instance], the quantity of general driver circuit output terminals [i.e. 3] being different than the quantity of remainder driver circuit output terminals [i.e. 2] (see Fig. 1(A) and Column 4, Lines 22-68 -- wherein S - (OP * (DC-1)) = 5 - (3 * (2-1)) = 5 - (3 * 1) = 5 - 3 = 2 = the quantity of remainder driver circuit output terminals = 2).

Regarding claim 26, Takeda et al. discloses each driver circuit of the plurality of driver circuits is separate and distinct from another driver circuit of the plurality of driver circuits (see Fig. 1(A)).

Regarding claim 27, Takeda et al. discloses the plurality of pixels is arranged in a two-dimensional matrix shape (see Fig. 2).

Regarding claim 28, Takeda et al. discloses the pixel includes a transistor [Fig. 2, 11-d], a gate electrode [Fig. 2, 11-a] of the transistor being electrically connected to the gate line, a source/drain of the transistor [Fig. 2, 11-b] being electrically connected to the signal line (see Fig. 2; Column 2, Lines 56-68).

Regarding claim 29, Takeda et al. discloses the plurality of gate lines is a plurality of rows and the plurality of signal lines is a plurality of columns (see Fig. 2).

Regarding claim 31, Takeda et al. discloses a surplus connecting region [Fig. 2; 12, 13, & 15] that does not contribute to the display portion [Fig. 2, 11] does not occur on the display (see Column 2, Line 56 - Column 3, Line 27).

Regarding claim 37, Takeda et al. discloses an output terminal of the plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch [Fig. 1(A), 32], the time-divisional switch providing a de-multiplexed signal potential to the signal line, the de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of the plurality of primary colors and supplied to the signal line (see Column 4, Lines 22-68).

Regarding claim 43, Takeda et al. discloses the plurality of primary colors is a first primary color, a second primary color, and a third primary color (see Column 2, Lines 55-68).

Regarding claim 44, Takeda et al. discloses the quantity of general driver circuit output terminals [i.e. 3, for instance] is greater than the quantity of remainder driver circuit output terminals [i.e. 2, for instance] (see Fig. 1(A)).

Regarding claim 45, Takeda et al. discloses the sum total of general driver circuit output terminals [i.e. 3, for instance] and the remainder driver circuit output terminals [i.e. 2, for instance] is equal to the plurality of signal lines [i.e. 5, for instance] (see Fig. 1(A)).

Regarding claim 46, Takeda et al. discloses the plurality of driver circuits include more than one general driver circuit (see Fig. 1(A)).

Regarding claim 47, Takeda et al. discloses each general driver circuit has an equal number of general driver circuit output terminals (see Fig. 1(A)).

Regarding claim 48, Takeda et al. discloses the plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which the display portion is formed (see Fig. 2; Column 2, Line 56 - Column 4, Line 6).

***Response to Arguments***

8. Applicants' arguments filed 20 August 2003 have been fully considered but they are not persuasive. The applicants contend the cited prior art of Takeda et al. (US 4,825,203) fails to teach the total number of signal lines being different than the number of output terminals. However, the examiner respectfully disagrees. Takeda explicitly illustrates a total number [Fig. 1(a), $N > 1$] of signal lines [Fig. 1(A), $Q_1$ to $Q_N$] being different than the number [Fig. 1(A), $n = 1$] of output terminals of each of the plurality of driver circuits [Figs. 1(A) & 2, 13 & $q_1$-$q_n$] (see Column 4, Lines 22-68).

The applicants additionally contend Takeda fails to teach at least one general driver circuit having a plurality of signal lines. However, the examiner respectfully disagrees. Takeda discloses at least one general driver circuit [Figs. 1(A), $q_1$ & $q_2$ working in conjunction] having a plurality of signal lines [Fig. 1(A), $Q_1$ & $Q_2$] (see Column 4, Lines 22-68).

Lastly, the applicants additionally contend Takeda fails to teach a remainder circuit having a plurality of output terminals. However, the examiner again respectfully disagrees. Takeda discloses a remainder circuit [Figs. 1(A), $qn_{-1}$ & qn working in conjunction] having a plurality of signal lines [Fig. 1(A), $Q_{N-1}$ & $Q_N$] (see Column 4, Lines 22-68).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

*Conclusion*

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
29 October 2003

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600